

## **Chapter 3**

# **Integrated Power Electronics Module**

### **3.1 Introduction**

To achieve high power density, low profile, the fundamental approach of electrical power processing is steadily moving toward high switching frequency. From previous analysis, high switching loss and high stress limited the ability to operate front end DC/DC converter at higher switching frequency.

From the history of power electronics, the technology improvements in power semiconductors have been the driving force for this problem. Moving from bipolar to MOSFET technology has greatly increased switching speed. For current semiconductor technology, very fast devices are available. For the power MOSFET used in front end application, they could be switched with mega hertz frequency range. The limiting factor now is the packaging technology. Because of the parasitic inductance and capacitance due to the packaging technology, the switching action has to be slowed down to limit the stress and undesirable noise problem. This limited the ability to reduce the switching loss of the devices.

For a typical front-end converter, individual power devices are mounted on the heat sink. Driver, sensors and protection circuits are implemented on a PCB, which is mounted close to power devices. The power devices are packaged with wire bonding technology. This kind of package has several limitations: first, the

parasitic related to the wire bond and PCB connection is very large; second, with wire bond technology, three-dimensional integration is not possible which limits the electromagnetic layout and thermal management. Some manufacturers have taken a more aggressive approach by integrate power semiconductors in die form on one common substrate with wire bonding. This approach provides some improvement by putting devices closer, but it doesn't resolve the limitations of traditional packaging technology.

Figure 3.1 shows the circuit diagram and switching waveform of a totem pole switches with interconnect parasitic considered with wirebond technology. When the MOSFET is switched at high current, those parasitic will introduce high stress on the devices. High voltage spike and ringing exists when turning off the switch. As switching speed increasing, the voltage overshoot will increase.

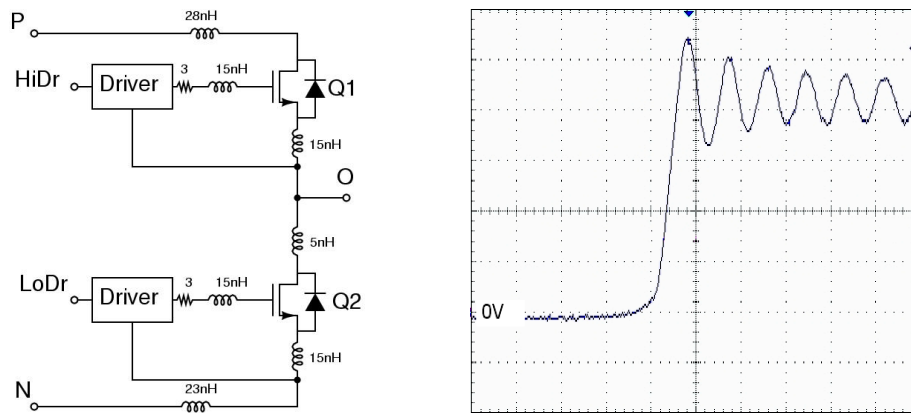


Figure 3.1 Totem pole switches with parasitic inductance and Q2 Vds (100V/div)

Another problem comes from the gate related parasitic. As shown in Figure 3.2, the gate driver loop shares  $L_s$  with power path. This will greatly impact the switching performance of switches. During turn off of upper switch Q1,  $L_s$  will

introduce a voltage  $V_{L_s}$  in the gate loop. This voltage will slow down the turn off speed thus introduce higher switching loss.

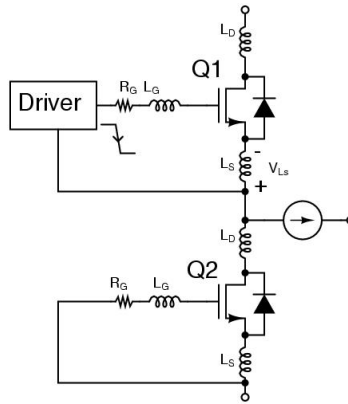


Figure 3.2 Impact of gate loop parasitic

Other than these electrical performance impacts of current packaging technology, thermal and noise problem will also greatly impact the capability of these technology for higher switching frequency.

From above discussion we can see, while power devices are still one of the major barriers for future power system development, it doesn't currently pose the fundamental limitations to power conversion technology. It is rather packaging, control, thermal management and system integration issues that are the major barriers limiting the fast growth of power conversion applications. To address these issues, advanced packaging technology is essential.

Another important issue for high power density is the packaging of passive components like magnetic and capacitors, which occupied biggest part of the system. With trend of low profile, planar magnetic is a must technology. With

planar magnetic, passive integration technique could be realized with high power density, low profile and better thermal performance.

In this part, the planar metalization device connection, which allows three-dimensional integration of power devices, and integration of power passives to increase the power density, as these dominate the physical size of the system, will be discussed.

### 3.2 Integrated Power Electronics Module for Front end DC/DC

Figure 3.3 shows a diagram for a front-end DC/DC converter for distributed power system with asymmetrical half bridge and current doubler configuration.

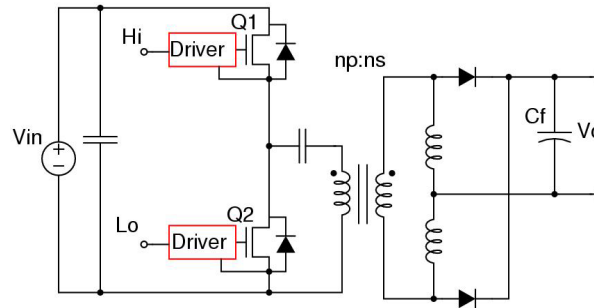


Figure 3.3 Schematic of front end DC/DC with asymmetrical half bridge current doubler

From previous discussion, we know that the parasitic inductance in the switching commutation path is important to the switching losses and the ringing amplitude. By integrating bare dies of switching devices together using planar integration technology, it can be expected that the parasitic inductance due to packaging be greatly reduced. To further reduce the impact of parasitic inductance, decoupling capacitor is needed. In discrete-component-based design,

the high frequency decoupling capacitor is paralleled with the DC link electrolytic capacitor and physically installed at the device terminals. By integrating the capacitor into the package, the interconnection from the capacitor to DC/DC switch is simplified and the decoupling effect is improved. Besides the concern of the parasitic inductance in the power path during switching commutation, the common source inductance between gate driver path and the main power path affects switching loss greatly too. During turn-off, the voltage drop on the common source inductance dynamically reduces gate voltage slew rate applied to the gate of MOSFET die, the switching speed is slowed down and this limits the switching loss reduction. Integrating the gate driver circuitry along with the devices further reduces the effective gate driver loop inductance.

In the front-end DC/DC converter, the size and dimensions of the passive components strongly affects the total size and volume of the converter. To achieve low profile of the converter, a planar magnetic component is always preferred. To further increase the power density and reduce the profile, there is a demand for the integration of passive components into one planar module, which is known as passive IPEM. The original work of an integrated inductor-capacitor structure led to the development of a planar technology to integrate inductors, capacitors and transformers (L-C-T) for resonant converter applications. The integration of passive components for PWM AHB DC/DC converter is another application of L-C-T technology for DC/DC converters.

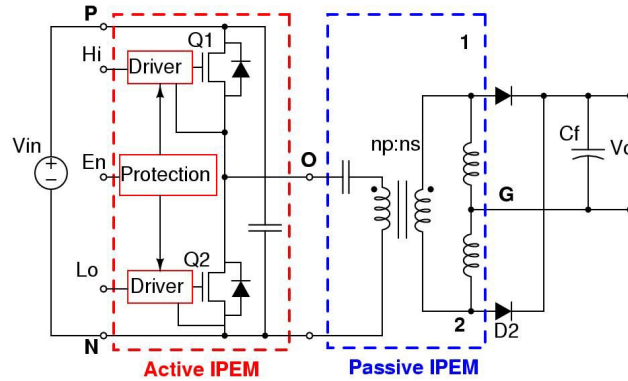


Figure 3.4 System partitioning of front end DC/DC converter

From above discussion, the front end DC/DC system could be divided into several blocks as shown in Figure 3.4. One block is the active switches and their drivers that include all the paths sensible to parasitic inductance. Another block is the passive components. With these two blocks, the most critical components for electrical performance and power density are included. Because of the different materials used for these blocks, it is difficult to integrate all these components into one module. Here two IPEMs are been identified and developed: active IPEM and passive IPEM.

### 3.2.1 Active IPEM

For active IPEM, our target is to develop a packaging technology, which provides three-dimensional planar packaging. With three-dimensional planar structure, low profile system could be achieved. Also, with real three-dimensional planar structure, thermal characteristic could be improved. As high switching frequency is our target for system design, lower parasitic is another important criteria for desired packaging technology. Several technologies were been

developed in CPES. They are Die Dimension Ball Grid Array, Dimple Array Integration, and Embedded Power technology.

Flip-chip-on-flex (FCOF) power switching stage modules consist of discrete power chip packages with some of the gate driver components. These chip packages are named Die-Dimensional Ball Grid Arrays (D2BGAs) that comprise a power chip, inner solder bumps, high-lead solder balls, and molding resin. Figure 3.5(a) shows a D2BGA package. The cross section of the package structure is illustrated in Figure 3.5(b). The chip-scale packaged devices are flipping soldered to a patterned flexible substrate. An organic underfill material is introduced into the gap between the packages and substrate to enhance mechanical adhesion and reliability by distributing stresses caused by the mismatched coefficients of thermal expansion between the chip and substrate. To complete the electrical circuitry and achieve good thermal performance, the backsides of the power chips are soldered on to a patterned direct bond copper (DBC) substrate. Finally, the power stage is encapsulated. The photo in Figure 3.5(c) shows a prototype of the packaged FCOF switching power stage module.

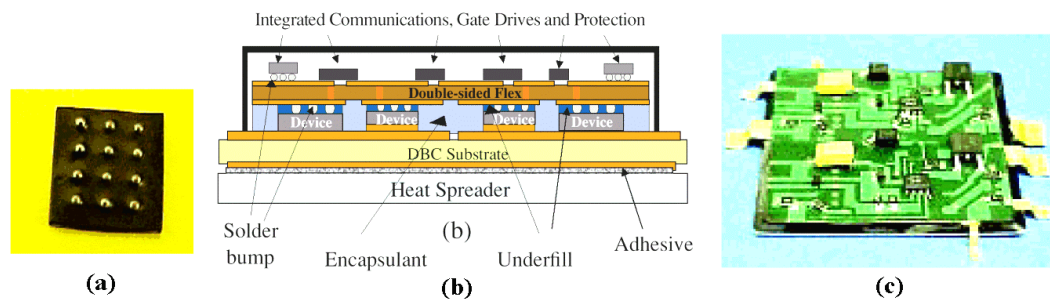


Figure 3.5 (a) D2BGA IGBT chip-scale package, (b) schematic of FCOF power switching stage module structure, and (c) FCOF power switching module prototype.

Aiming at enhancing thermal fatigue reliability of solder bumping interconnects in power packaging applications, we have developed the Dimple Array Interconnect (DAI) technique. DAI packaging involves the use of copper flex/sheet with arrays of preformed dimples, which serve as both electrical interconnections and heat removal paths. As shown in Figure 3.6(a), the key feature of DAI is its dimpled metal interconnects, which are convex valleys on metal sheet protruding from one side, that enable easy forming of solder joints with underlying devices. The resultant smooth fillets in solder bumps could significantly reduce thermally induced stresses and strains. An integrated DAI power switching stage module is schematically shown in Figure 3.6(b). The DAI module is realized by solder-attaching DAI power devices, such as diodes and IGBTs, onto DBC substrate, followed by underfilling and encapsulation. Because only one type of solder is needed to form the dimple solder joint, there are more options to select a solder of different melting temperatures for the surface mount (SMT) gate driver and control components. The prototype Dimple Array Interconnect Power DAI power switching is shown in Figure 3.6(c).

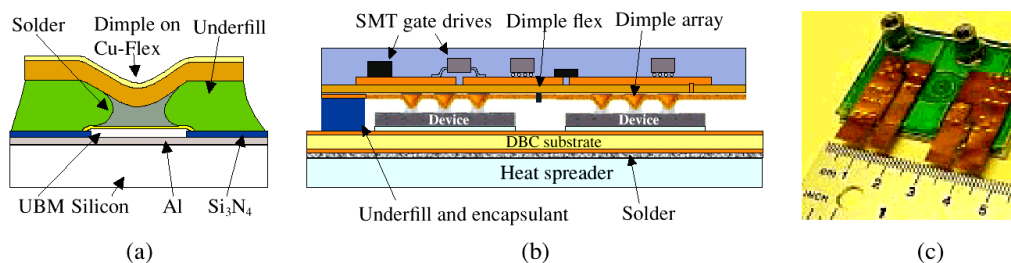


Figure 3.6 (a) Schematic of Dimple Array Interconnect, (b) integrated DAI power switching stage module, and (c) prototype Dimple Array Interconnect power switching stage module.



Embedded power technology has been developed for integrated packaging of integrated power electronics modules (active IPEMs), which are usually comprised of power switches and associated electronics circuitry. Figure 3.7(a) shows the conceptual structure of the embedded power packaged module. It consists of three levels: electronic components, a multiple embedded power chip stage, and a base substrate (from top to bottom). These three parts are soldered together to build a final module. The electronics circuitry includes a gate driver and control and protection components. The base substrate provides electrical interconnection and cooling of power chips. The core element in this structure is the embedded power stage that comprises the ceramic frame, power chips (silicon in the figure), isolation dielectrics and metalized circuit. Inside the power stage, multiple bare power semiconductor dies, featuring vertical semiconductor structures with topside and backside electrode pads, are directly buried in a ceramic frame. Table I summarizes the fabrication steps of an embedded power module. They are the ceramic cutting, device mounting, dielectric printing and metalization. One of the features of this technology is its mask based processing. The metalized base substrate is patterned using photolithography, the dielectric polymer is applied with a screen-printing method, and the chip-carrier ceramic frame is fabricated by computer controlled laser machining.

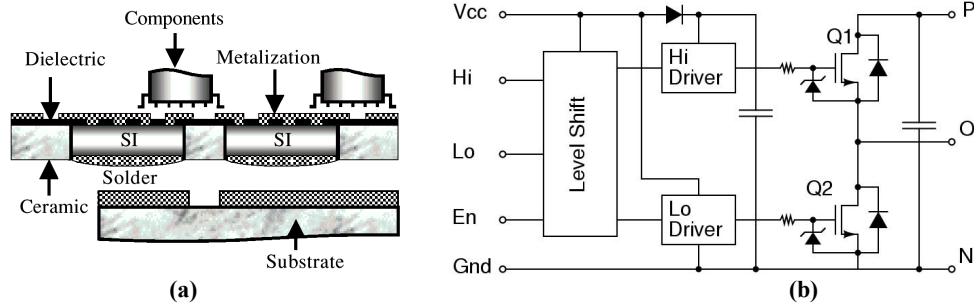


Figure 3.7 (a) Schematic integration structure of embedded power module and (b) circuit diagram

Compare these three technologies; first two technologies are still based on traditional packaging concept with different interconnection method. Embedded power technology is one step further in three-dimensional packaging, which is a true planar structure with compatible process as planar integration technology. It is used to build the IPEM for distributed power system.

Figure 3.7(b) shows the schematic diagram based on the totem-pole structure with high- and low-side drivers and control. The half-bridge consists of two MOSFET devices and gate drivers using three ICs. Figure 3.8 depicts the assembly processes following the embedded power stage and the final packaged module. Figure 3.8(a) and (b) present the top and bottom views of the embedded power stage. Figure 3.8(c) shows components mounted on the topside of the metalized pattern. An Al<sub>2</sub>O<sub>3</sub> DBC substrate with 10mil-thick Cu on both sides of 25 mil-thick ceramic was used as the base substrate, which was pattern etched on one side (Figure 3.8(d)), while the other side is attached directly to the heat spreader. Figure 3.8(e) shows the power stage solder-mounted to the substrate. Finally, after the gate driver had been mounted and connected to the power stage,

the entire module was encapsulated with protruding input/output pins (Figure 3.8(f)). The completed module measures 30x27x10mm.

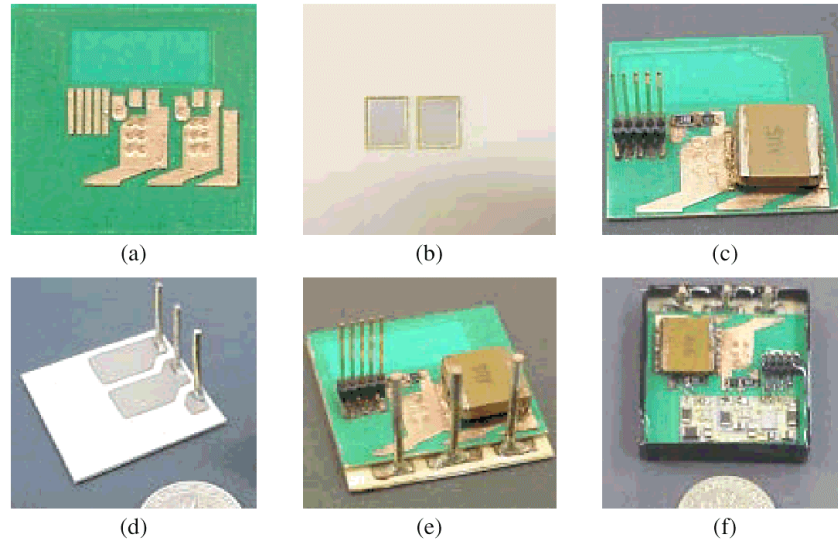


Figure 3.8 Assembly process of embedded power module: (a) top view of embedded power stage, (b) back view of embedded power stage, (c) components attachment on top, (d) patterned DBC for base substrate, (e) soldered on substrate, and (f) final encapsulated module.

### 3.2.2 Passive IPEM

In order to integrate the electromagnetic power passive components into modules, passive integration technology was developed. The technology can be best described by first considering a simple bifilar spiral winding as shown in Figure 3.9. This structure consists of two windings (A-C and B-D), separated by a dielectric material. This resultant structure has distributed inductance and capacitance and is best described as an electromagnetically integrated LC resonant structure for which the equivalent circuit characteristics depend on the external connections. With more winding layers, more complex integrated structures can be realized. This has been demonstrated with an integrated structure

as shown in Figure 3.9. With this technology, the classical term “parasitic” therefore no longer applies and all the higher order impedances are rather referred to as structural impedances. This technology mostly been implemented in resonant converter applications. Here, it is also been used in the asymmetrical half bridge front end DC/DC converter. In this application, the planar passive integration technology, together with planar integrated magnetic technology, were combined to integrated all the high frequency passive components.

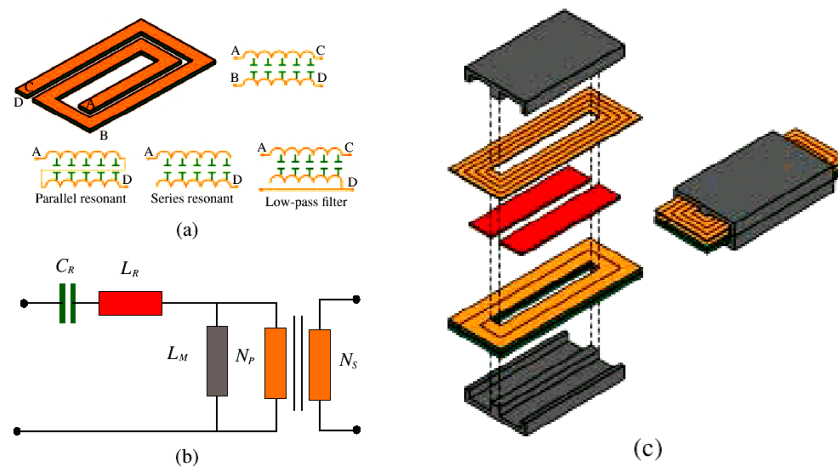


Figure 3.9 (a) Spiral integrated LC structure with distributed capacitance and possible external connection configurations, (b) simplified equivalent circuit, and (c) exploded view.

For asymmetrical half bridge converter, two integration steps are used to integrate all the passive components except output filter capacitor into one structure.

The schematic of the passive components in asymmetrical half bridge with current doubler is shown in FIG. There are two filter inductor, two transformers, and one DC blocking capacitor. Integrated magnetic concept could be used to

integrate all the magnetic components into one magnetic structure. This integrated is realized as shown in FIG. It is discussed in detail in [C17][C18][C20]. With two E cores, the two transformers could be constructed on the two outer legs. Its magnetizing inductance is used to build the filter inductors.

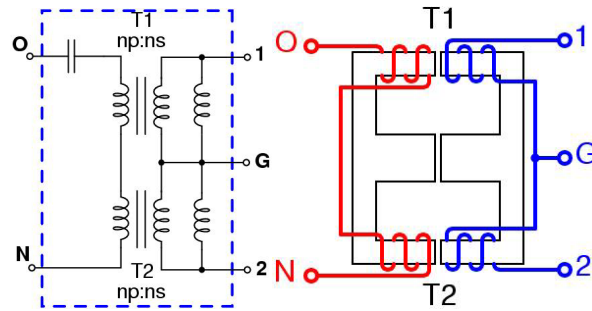


Figure 3.10 Magnetic integrated for asymmetrical half bridge converter

As low profile is another important aspect for front end DC/DC converter development, planar magnetic design is preferred to reduce passive components profile. FIG shows the design of planar integrated magnetic. It is built with two planar E cores and one I core. In this structure, I core has the same function as the center leg in previous design.

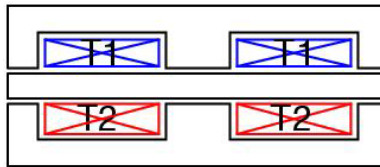


Figure 3.11 Planar integrated magnetic for current doubler rectifier

With planar integrated magnetic, next the passive integration method will be applied to integrate the DC blocking capacitor into the structure. As shown in FIG, the DC blocking capacitor is implemented in transformer  $T_1$  by using the

hybrid winding technology, The hybrid winding is implemented using copper traces on both sides of the winding and a dielectric layer placed in the middle to enhance the capacitive component of the winding. The transformer  $T_2$  is implemented according to conventional planar low-profile transformer technology. The inductances of the current doubler are realized by the magnetizing inductances of both transformers. Figure 3.12 shows a picture of the final passive IPEM implemented for the AHB DC/DC converter.

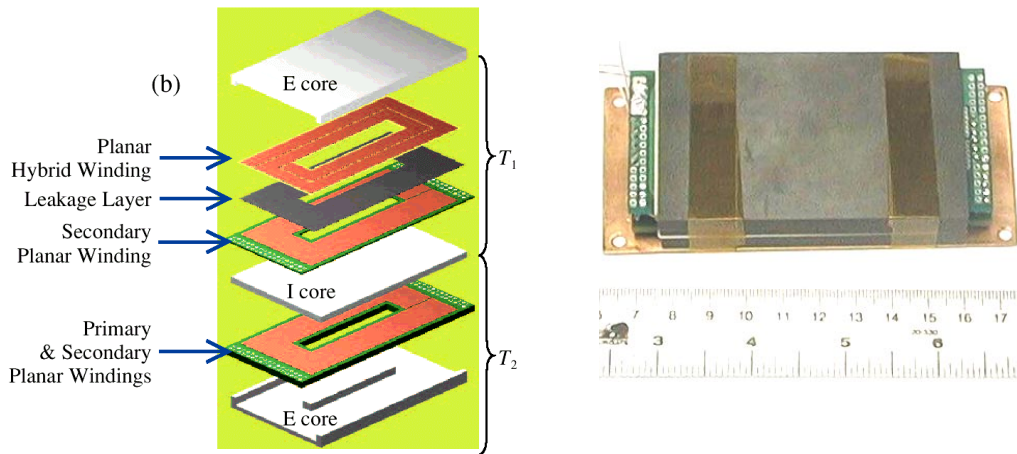


Figure 3.12 Exploded view and photo of passive IPEM

### 3.3 Performance evaluation

With the use of IPEMs, the front-end converter design takes advantage of the modular design. Besides to the benefit of easy assembly and the reduced overall volume, the active IPEM itself also offers electrical performance improvements, such as the switching loss reduction and the lower voltage stress. Since it is difficult to directly measure the losses in the devices after being installed in the

converter, the simulation based on Saber<sup>TM</sup> is used to analyze the effects of the parasitic reduction in the front-end converter.

To build the simulation model, the device models for the power devices are first verified. Saber<sup>TM</sup> provides the modeling tool for the power MOSFETs and some manufacturers provide the model for some devices. However no any manufactures guarantee the accuracy of their models. Therefore efforts must be taken to verify the model accuracy for the expected operating conditions. Since the switching stress and losses are of major concern, the gate charge and the V/I characteristics are obtained in simulation to compare with the data sheet. As shown Figure 3.13 and Figure 3.14, the model matches the data sheet quite well.

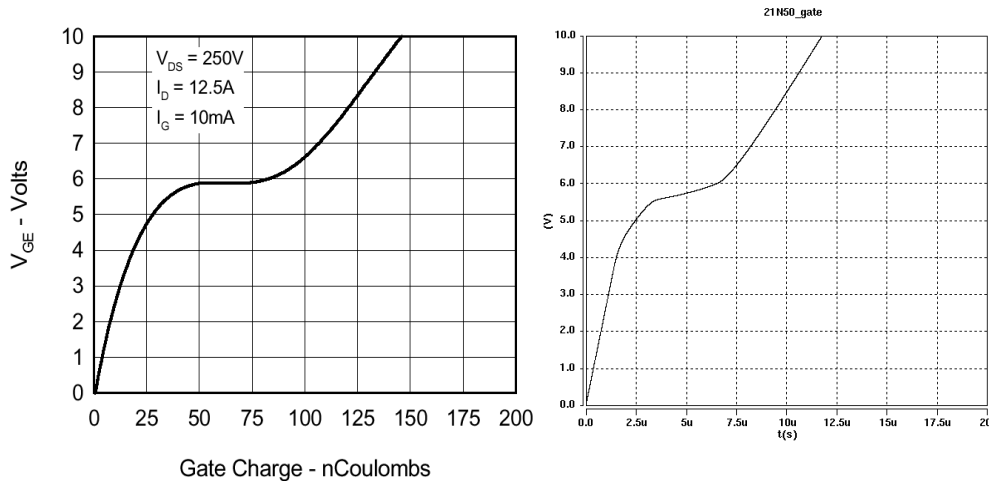


Figure 3.13 Gate charge curve of IXFH21N50 (a) Datasheet, (b) simulated

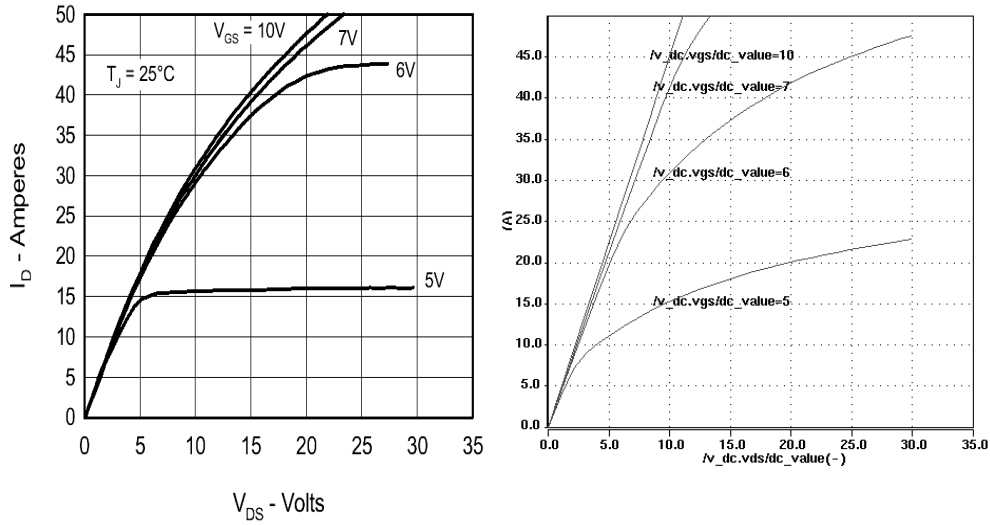


Figure 3.14 V/I characteristic of IXFH21N50 (a) datasheet and (b) simulated

Next, the parasitic parameters of discrete approach and IPEM are extracted based on the impedance measurement method. The resultant parasitic inductance is shown in Figure 3.15. Compare these two models: first all the parasitic inductances are greatly reduced; second, in active IPEM, the gate loop doesn't share inductance with power loop. These two aspects will provide significant improvement on electrical performance.

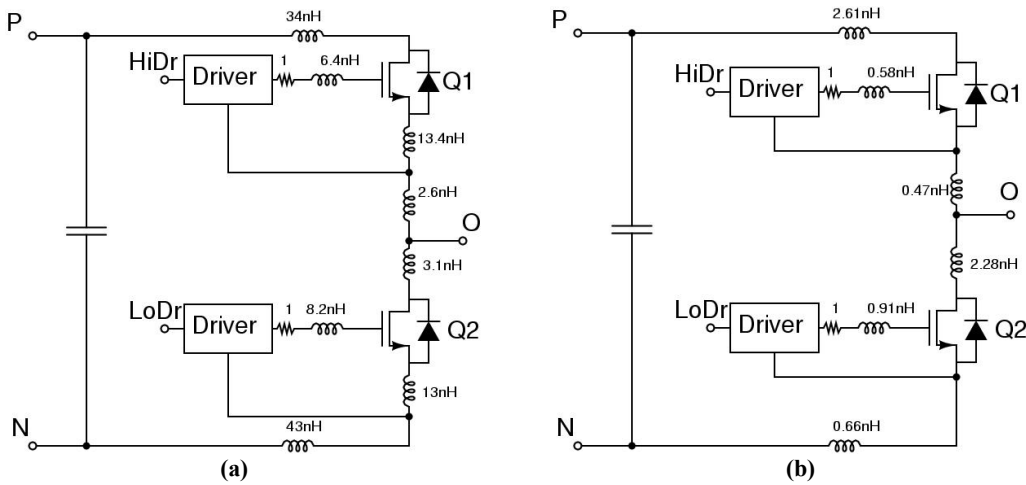


Figure 3.15 Parasitic of (a) discrete MOSFET and (b) Active IPEM



The switching circuit for the active IPEM and the discrete components is built, which includes the parasitic inductances inside the device package and gate driver circuitry. The gate driver pulse is set as ideal square waveform. At 1kW power level, the peak switched current is about 10A. Figure 3.16 shows the simulated waveform of drain source voltage. With active IPEM, the voltage overshoot is reduced to 416V compared with 465V for discrete version. The turn-off loss is reduced from 48uJ to 25uJ by using IPEM. Considering 200kHz operation of DC/DC converter, the turn-off loss is reduced by 8W with 4ohm gate resistance. This translated into about 1% efficiency increase of the front-end converter and 10% loss. Figure 3.17 and Figure 3.18 shows the improvements of active IPEM for different gate resistance.

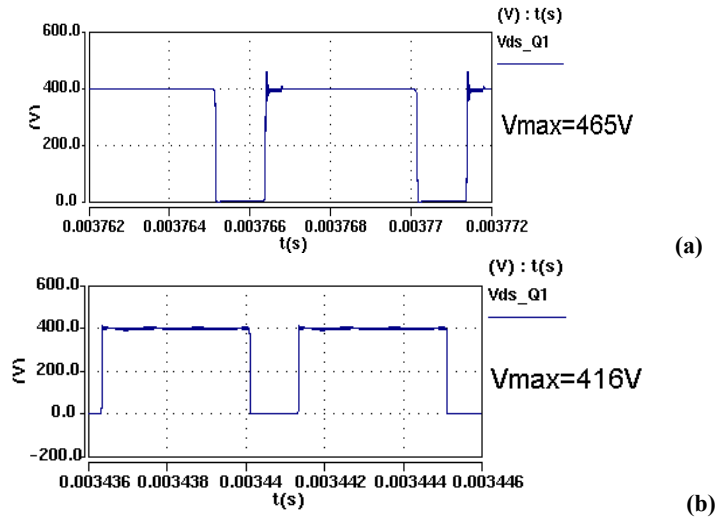


Figure 3.16 Simulation waveforms of Q1 drain source voltage (a) Discrete, and (b) IPEM

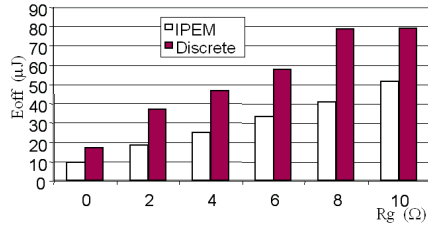


Figure 3.17 Active IPEM turn-off loss reduction

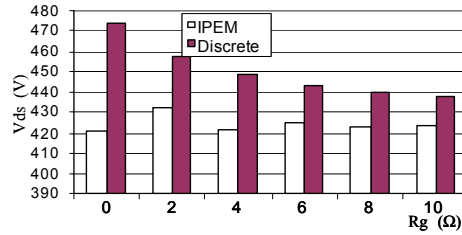


Figure 3.18 Voltage overshoots improvement by IPEM

With passive IPEM, all the passive components except output filter capacitor are integrated into one single package. This could greatly reduce the volume of passive components. Another benefit is from planar design. With planar structure, thermal characteristic of the passive IPEM is improved significantly compared with traditional magnetic structure. In following part, three prototypes were built and compared. They are shown in Figure 3.19. All three prototypes are asymmetrical half bridge with current doubler. First prototype is based on discrete passive design. Second prototype use integrated magnetic technology. Third prototype is built with passive and active IPEM. With discrete passive components, the total volume of passive components is  $343\text{cm}^3$ . By applying integrated magnetic concept, it is reduced to  $258\text{cm}^3$ . With passive IPEM, all the passive components except output filter capacitors are integrated. A volume of  $87\text{cm}^3$  is achieved, which is five times improvement as shown in Table 3-1.

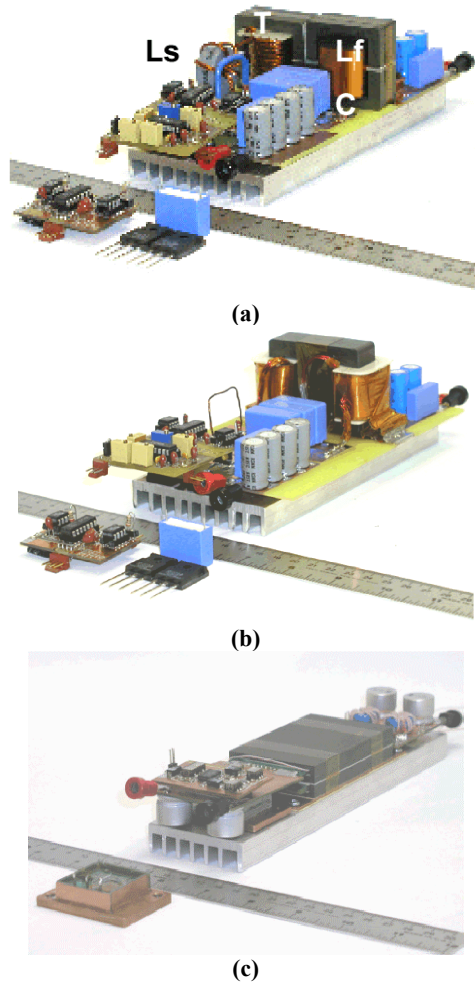


Figure 3.19 Photos of three prototypes to be compared (a) discrete design, (b) integrated magnetic design and (c) Passive IPEM design

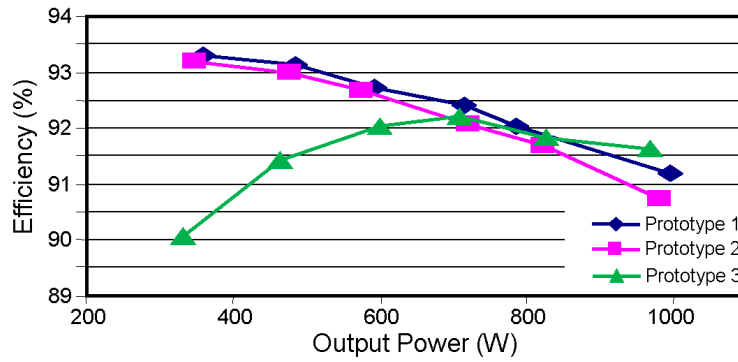


Figure 3.20 Test efficiency of three prototypes

Table 3-1 Comparison of three prototypes

<b>Parameters</b>	<b>Prototype 1</b>	<b>Prototype 2</b>	<b>Prototype 3</b>
No. of passive components	6	4	1
Volume of passive components (cm <sup>3</sup> )	173	151	82
No. of terminals	15	12	5
Volume of terminals (cm <sup>3</sup> )	170	107	5
Total passive volume (cm <sup>3</sup> )	343	258	87
System Profile	2U	2U	1U
System Power Density	1	X1.2	X3.6

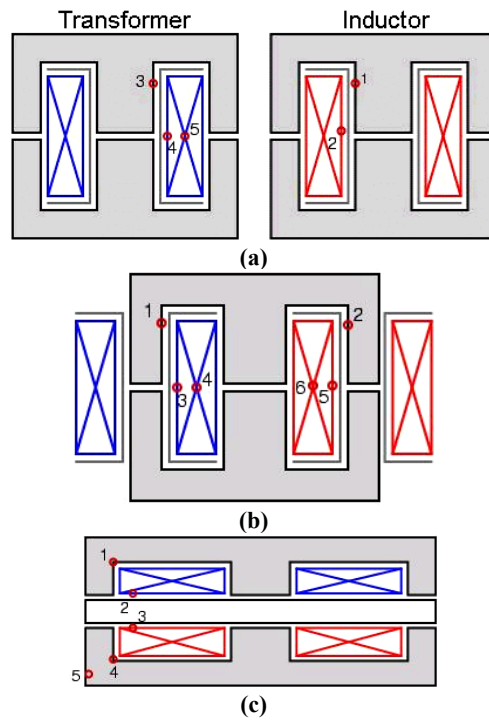


Figure 3.21 Temperature test setup for three prototypes

Table 3-2 Temperature test results of three prototypes

<b>Temperature</b>	<b>1( °C)</b>	<b>2( °C)</b>	<b>3( °C)</b>	<b>4( °C)</b>	<b>5( °C)</b>
Prototype 1	39.8	54.3	74.1	77.3	79.1
Prototype 2	75.4	54.9	109.2	106.5	79.3
Prototype 3	63.7	71.7	71.9	67.2	65.2

Another benefit from passive IPEM is improvements on thermal characteristic. These three prototypes are tested. Figure 3.21 shows the test setup. For each structure, 5 thermal couplers are embedded into the structure. Table 3-2 shows the test results. Compare these three prototypes, one significant improvements of IPEM is the uniform distribution of temperature, which means better thermal characteristic. For discrete version, with more material, although the lowest temperature is lower, hot spot shows even higher temperature than passive IPEM. With integrated magnetic design, the volume is reduced, but hot spot temperature is much higher than discrete version. With passive IPEM, the structure volume is reduced by 5 times; at the same time the temperature is even lower than the discrete version.

### **3.4 Summary**

In this chapter, the advanced packaging for front end DC/DC converter is discussed. To achieve high power density and low profile, high switching frequency is necessary. Currently, the power MOSFET could be switches at very high frequency. The high stress and loss limited the ability to use these devices at high switching frequency. These problems are mainly caused by the parasitic components in the circuit. Thermal management also imposes a limitation on the power density achievable with current packaging technology.

Two IPEMs are identified for front end DC/DC converter: active IPEM and passive IPEM. Active IPEM mainly focused on the improvements on parasitic

and thermal issues, while passive IPPEM is focused on improved the power density of passive components with advanced passive integration technology.

With embedded power technology, two switches in totem pole configuration, gate driver and filter capacitor are integrated with planar 3D packaging. With active IPPEM, the parasitic inductance is reduced to less than 10% or discrete devices. With reduced parasitic, voltage stress and switching loss are significantly reduced.

Passive IPPEM is constructed with combination of different technologies: integrated magnetic, planar magnetic and passive integrate technologies. With passive IPPEM, three passive components: transformer, filter inductor and DC blocking capacitor, are integrated into one single package. With passive IPPEM, the power density of passive components is improved by 5 times. At the same time, thermal characteristic is significantly improved. The temperature in the passive structure is uniformly distributed.

With active IPPEM and passive IPPEM, the power density and profile of the front end DC/DC converter are improved.